

Appl. No. 10/064,597
Amdt. dated April 15, 2005
Reply to Office action of February 23, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 1 (currently amended): A method for decoding instructions in an execution package with
5 a processor, each instruction comprising an identification segment and an instruction
segment, the method comprising:
using an assembler to assemble instructions into different execution packages;
using the assembler to reorder the instructions by separating identification segments
from instruction segments, grouping all identification segments of the
10 execution package together, and grouping all instruction segments of the
execution package together; and
using the processor to decode identification segments of the instructions at the same
time.
- 15 2 (original): The method of claim 1 wherein the identification segments include data
specifying lengths of corresponding instruction segments.
- 3 (original): The method of claim 2 wherein each identification segment includes
information to indicate whether an instruction corresponding to the identification
20 segment is a last instruction in the execution package.
- 4 (original): The method of claim 3 wherein a length of each identification segment is
added together to calculate a total length of the execution package.
- 25 5 (original): The method of claim 1 wherein number of instructions in an execution
package is less or equal to number of instructions that the processor can execute at
the same time.

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6 (original): The method of claim 1 wherein the instructions are variable length instructions.

7 (original): The method of claim 1 wherein the processor is a digital signal processor
5 (DSP).

8-9 (cancelled).

10 (original): A method for decoding instructions in an execution package with a
10 processor, each instruction comprising an identification segment and an instruction
segment, the method comprising:
using an assembler to assemble instructions into different execution packages;
using the assembler to reorder the instructions by separating identification segments
from instruction segments, grouping all identification segments of the
15 execution package together, and grouping all instruction segments of the
execution package together;
using the processor to decode identification segments of the instructions at the same
time; and
adding a length of each identification segment together to calculate a total length of
20 the execution package.

11 (original): The method of claim 10 wherein the instructions are variable length instructions.

25 12 (new): The method of claim 10 wherein number of instructions in an execution
package is less or equal to number of instructions that the processor can execute at
the same time.

13 (new): The method of claim 10 wherein the processor is a digital signal processor

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(DSP).